3

Research Trend in LSI Technologies — Report on Presentations at the VLSI Symposia and the Silicon Nano-electronics Workshop —

TETSUYA YAMAZAKI
Information and Communications Research Unit

3.1 Introduction

The annual "VLSI Symposia" ("VLSI Symposia on Technology and Circuits") and "Silicon Nano-electronics Workshop" (hereafter "Nano-electronics Workshop"), both of which are among major international conferences on LSI technologies, were held in Hawaii, US, in mid-June this year. The two conferences have been organized by the IEEE and annually held by Japan and the US in turn.

The VLSI Symposia consist of the "Symposium on VLSI Technology" (hereafter "Technology Symposium"), which concerns device technologies, and the "Symposium on VLSI Circuits" (hereafter "Circuit Symposium"), which discusses circuit technologies. Both symposia cover the latest technologies currently in use and those technologies under development for 1 to 2 generations ahead (for this year's events, 130nm to 65nm generation). Presentations are made mostly by private enterprises. This year, there were 86 presentations (of them, 2 were keynote speeches) for the Technology Symposium and 88 (4 were keynote speeches) for the Circuit Symposium. Combined, the participants totaled approx. 600 people.

The Nano-electronics Workshop focuses on more futuristic technologies. This conference is important since it may indicate a course of direction for future LSI technologies. Most presentations are given by universities. This year, there were 56 presentations (of them, invited research papers accounted for 6 and posters 27), and the participants amounted to approx. 200 people.

This report will explain some of the topics of these international conferences.

3.2 This year's trends

3.2.1 VLSI Symposia

(1) Technology Symposium

It has long been pointed out that simple scaling (i.e., miniaturizing device structures to increase integration and operating speed) is nearing its limit. New device structures, such as high-dielectric constant (High-k) gate insulation film*1, low-dielectric constant (Low-k) insulation film*2 and SOI (Silicon on Insulator)*3, are attracting much attention and some of them have already been commercialized. At this year's symposium, a total of 16 presentations were made concerning the high-dielectric constant (High-k) gate insulation film. Concerning the material for the film, silicon oxynitride (SiON) is the leading candidate for the immediate future, while hafnium oxide (HfO_2) is the potential candidate for the 65nm generation or later, and there were a large number of presentations on these two subjects. However, High-k gate insulation films share a major drawback in common: their carrier mobility, which directly affects the working speed of a transistor, is lower than conventional SiO_2 gate insulation films. The solution to this problem is nowhere in sight, and this disadvantage has been a stumbling block to commercializing High-k gate insulation films.

This year's symposium has a new session concerning the strained Si structure, which attracted attention at last year's Nano-electronics

Workshop (see "Science & Technology Trends-Quarterly Review" No.2 and No.4), and there were 4 presentations on this subject. In addition, IBM presented a device that used a High-k gate insulation film and the strained Si structure in the highlight session. (also see the July 2002 issue of "Science & Technology Trends", Topics part)

Another characteristic of this year's symposium was that those presentations on SoC (System on Chip, which integrates a processor, memory and analog circuits onto a single chip), non-volatile memories, analog devices and high-frequency devices gained much attention as a reflection of the fact that mobile devices have become widespread and have improved their performances, and the wireless LAN market has begun to expand. In contrast, there were fewer presentations on "DRAM Technology" sessions, indicating that the status of DRAMs as a technology driver has lowered.

Concerning the next-generation lithography*4, which will be the key to miniaturization, there were presentations on F_2*4 and EPL (Electron Projection Llithography)*4. However, it has been questioned whether equipments, masks and processes will be developed in time for the 65nm-generation LSI (expected to be mass-manufactured from around 2007). Therefore, a presentation on a mask technology that may prolong the life of ArF*4 — used in 130nm to 100nm generation — into the 65nm-generation LSI, drew considerable attention. This will be discussed in the next chapter.

(2) Circuit Symposium

Presentations on SoC also attracted attention in the Circuit Symposium. In addition, as for non-volatile memories, those presentations on the current mainstay multi-thresholding technology for flash memories (i.e., storing multi-bit signals in a single memory cell), and the next-generation memories such as the magnetic memory (MRAM)*5 and the ferroelectric memory (FeRAM)*5, attracted much attention.

Other notable presentations included those concerning low power consumption technologies. Low power consumption is an important performance indicator for mobile devices and home electric appliances. And the problem of heat generation that increases in conjunction with intensified integration and speeding up is becoming serious even for high-performance devices like PC processors. There was a heated debate in a panel discussion on this problem. At the panel discussion, Mr. Mizono of NEC pointed out that since each chip has a heat generation limit, the speed of performance increase would be almost halved from the current 3 folds per generation. Although measures to cope with this problem were suggested, such as specially designed packages and transistors and cooling methods, there seems to have been no decisive measure. Mr. Ito of Hitachi stressed that new concepts should be developed such as a processor based on a memory architecture.

In the keynote speeches, MEMS*6 was mentioned in both the Technology Symposium and the Circuit Symposium. In the Technology Symposium, Dr. Esashi of Tohoku University, and in the Circuit Symposium, Dr. K.D. Wise of the University of Michigan, gave presentations. In particular, Dr. Wise indicated the application in an implant treatment device with which a MEMS chip is implanted into the human body. The chip comprises medication delivery systems, sensors and controllers. The chip size is 0.5mm square or less, it receives power from a source outside the body via an microwave. Since it can control muscles by electrically stimulating nerves, studies are being conducted on the application of the chip for patients with malignant nervous diseases such as Parkinson's disease.

3.2.2 Nano-electronics Workshop

What became the center of attention in this year's Nano-electronics Workshop as a future technology that follows the strained Si structure was a transistor having a 3D structure called "FinFET." It will be discussed in detail in Chaper 3.4.

Concerning technologies in the nano-tech category, those presentations using highly feasible structures for devices, such as quantum dots, were especially notable. By contrast, there was only one invited speech given by IBM regarding the carbon nano-tube transistor. Since most of these nano devices operate only at ultra-low temperature, how to design nano devices that can operate at room temperature was hotly debated. It seems

Table 1: Roadmap for LSI sizes and lithography in ITRS2001

	2001	2002	2003	2004	2005	2006	2007	2010
DRAM 1/2 pitch	130	115	100	90	80	70	65	45
MPU 1/2 pitch	150	130	107	90	80	70	65	45
MPU Physical Gate Length	65	53	45	37	32	28	25	18
Optical lithography	ArF					F_2		EPL EUV

(Unit : nm)

Source: Author's compilation based on ITRS2001 (International Technology Roadmap for Semiconductors, 2001 edition), etc

that it will take much more time before this problem is solved.

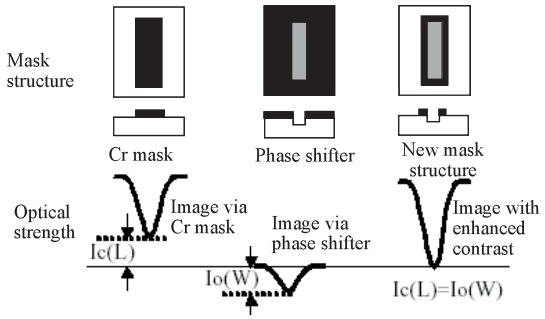
3.3 Next-generation Lithography

According to the latest roadmap for lithography (Table 1), which is the key to miniaturization, F_2 represents the 65nm generation and the electron projection lithography (EPL) or the extreme-ultra violet ray lithography*4 (EUV) represents later generations. However, since F_2 lithography devices will likely be only effective for the 65nm generation and because of technological difficulties, western semiconductor manufacturers including Intel are shifting to EUV (see April 2001 issue of "Science & Technology Trends"). These movements seem to be also affecting Japanese semiconductor manufacturers.

At this year's event, Selete*7 demonstrated that development resist for F_2-Lithography had been under way. In the meantime, Matsushita pointed out that EPL was superior to ArF and F_2 in focal depth and resolution. Matsushita also presented a mask technology for prolonging the life of ArF (used for the 130 to 100nm generation) for the 65nm generation, and attracted much attention (Figure 1). It is a kind of resolution enhancement technologies having a phase-shifting (shifting 1/2 light wave length) area in the middle of a printed pattern, thus to interfere with the surrounding lights; this technology is said to improve the focal depth and resolution as required for the 65nm generation even with an ArF lithography equipment. And, it is also notable that unlike conventional phase-shifting masks that can be applied only for repeated patterns (inverting the phases of adjacent patterns and enhancing the contrast using the interference), this technology can be applied even to isolated patterns.

Concerning the F_2 lithography, ASET*8 presented its research findings this June to point out that although the development of laser, mask materials and resists has been proceeding, there are still problems such as difficulties in mass manufacturing calcium fluoride lens*9, weakness of pellicle material that protects mask, and long-term durability against the burning of a contaminant. As for EPL and EUV, it is presently uncertain whether the development of masks and processes will be completed in time, and the prolongation of ArF's life is becoming the leading candidate for the next-generation lithography in terms of reducing the growing cost. By the way, in Japan, a total of 10 companies launched the Extreme Ultraviolet Lithography System Development Association (EUVA) this May in order to commercialize EUV for the 45nm and later generations.

Figure 1: Contrast enhancing technology presented by Matsushita



With a pattern having a line width below the wavelength, the image is blurred due to optic diffraction (left). The phase of light that passed the phase shifter is inverted with that of surrounding lights (center). When synthesizing both, the blurred area is compensated and the pattern contrast is enhanced (right).

Source: Author's compilation based on A. Mikasa et al., the "2002 Symposium on VLSI Technology Digest of Technical Papers," p. 200 (in 2002), etc.

3.4 Next device structure — FinFET

What gained much attention at the workshop as the next-generation technology following the strained Si structure was the FinFET structure. FinFET is a 3D structure in which the gate electrode is positioned around a channel (a transistor's part where an electric current passes) formed like a thin fin (see Figure 2). It is expected that FinFET will achieve faster operation, greater ON-stage current and less leakage current (less power consumption) than the current planar structured transistor. In addition, FinFET allows the creation of a finer transistor than the smallest possible size with lithography through the refined process. Dr. C. Hu from TSMC of Taiwan (the inventor of FinFET who also serves as a professor at UC Berkeley), who delivered an invited speech, demonstrated the properties of a FinFET prototyped at TSMC. He also stated that leading companies including IBM, Motorola and AMD are currently studying similar structures, and FinFET is among the leading candidates for the transistor structure in and after 2010.

TSMC also gave a detailed presentation on a FinFET with a gate length at 35nm (equivalent to the 65nm generation) in the VLSI Symposia. The presentation indicated that FinFET would demonstrate adequate performance even without introducing new materials like a High-k gate insulation film. Also, Motorola gave a presentation on FinFET's basic properties at the workshop.

FinFET has one drawback: its channel is too narrow to allow sufficient electric current. However, Dr. Hu showed a structure that allows sufficient electric current by forming multiple channels in a single transistor.

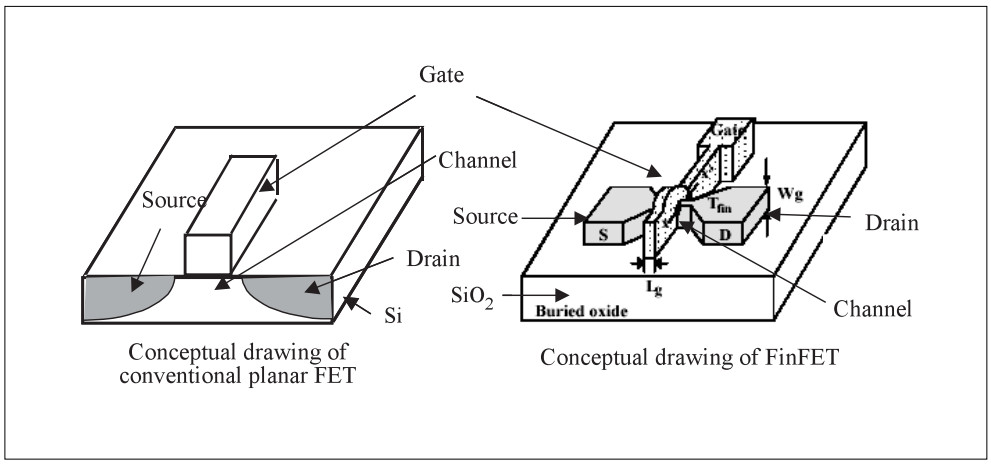
In contrast, a few presentations were delivered indicating that with the conventional planar FET, the surface roughness of the gate disturbed the travel of electric charge degrading the FET's performance. With the FinFET structure whose fin is formed by etching, it is anticipated that the roughness of the gate surface will be greater than that of the planar FET. This may become a problem in the future.

3.5 Research and development trends by country

In closing, this section will briefly analyze research and development trends by country in terms of the number of papers presented at the conferences. Table 2 shows the numbers of papers at each conference by country and region. These numbers include that of invited speeches, keynote speeches and poster sessions, but exclude panelists at panel discussions.

At both symposia, Japan and the US represented almost the same numbers. Given that the share of the Japanese semiconductor industry on the recent international market is dropping, and that the symposia were held in the US, it can be said that Japan made a good showing. South Korea ranked third to outperform Europe, and Taiwan also raised its presence. The 3 papers in the row

Figure 2: FinFET and conventional planar FET



Source: Author's compilation based on R. Yang et al., "2002 Symposium on VLSI Technology Digest of Technical Papers," p. 104 (in 2002), etc.

Table 2: Numbers of papers by country/region

Country/region	Technology Symposium	Circuit Symposium	Nano-electronics Workshop	Si Nano-electronics Workshop in 2001
Japan	35	37	8	18
US	32	42	25	6
Europe	8	2	9	7
South Korea	12	5	10	5
Taiwan	4	2	2	0
China	0	2	0	0
Other	1	3	0	0

Note: Overlapping papers through joint presentations are included.

Source: Author's compilation based on the proceedings of the conferences.

marked "Other" for the Circuit Symposium indicate theses presented by Canadian universities, and Canada has established a certain position in the field of circuit technologies.

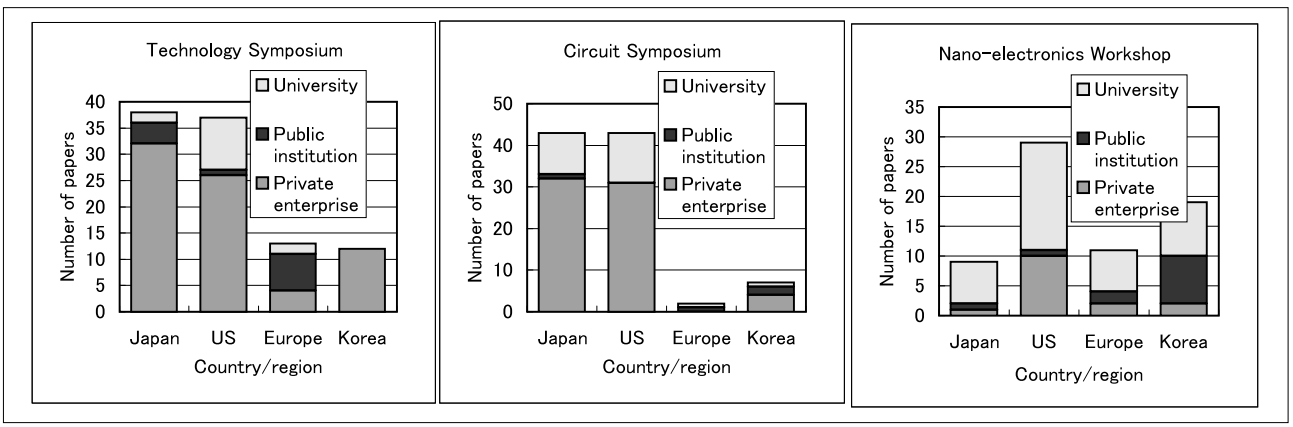
However, for the Nano-electronics Workshop, there were fewer Japanese papers than other major countries. This is due to the symposia's characteristic that the event is held by the US and Japan in turn, and every year the number of the host country's papers is much greater than that of the other. On the other hand, South Korea ranked second superceding Europe and Japan. This indicates that research activities in future technologies have also become more vigorous in South Korea. For reference, figures (numbers of papers by county and region) for the 2001 conference, held by Japan, are added to Table 2.

Figure 3 shows the numbers of papers presented by the top 4 countries/region for each conference. In these graphs, joint-research organizations each involving multiple companies, such as Selete of Japan and IMEC*10 of Europe, are categorized as "public institutions."

It is clearly indicated in the graphs that the two symposia were mostly represented by private enterprises, while the Nano-electronics Workshop was accounted for mainly by universities.

The Circuit Symposium graph indicates that Japanese universities made a strong showing. In the Technology Symposium, however, there was actually only one presentation by a Japanese university (one of the two presentations was a keynote speech). This was partially because it was held in the United States, but the fact that there are fewer universities in Japan that have facilities necessary for research into cutting edge devices is probably another reason. In fact, US universities represent a majority number of papers just because a limited number of universities equipped with important facilities made a large number of presentations. The reason for the large proportion of European public institutions is that IMEC and

Figure 3: Numbers of papers at each conference by institution



Note: Overlapping papers through joint presentations are included.

Source: Author's compilation based on the proceedings of the conferences

French CEA*11 made presentations in the form of joint research and the likes.

In the Nano-electronics Workshop graph, public institutions from South Korea represent a large proportion. In particular, a combination of ISRC (Inter-University Semiconductor Research Center) and Seoul National University accounted for most of those presentations. Of the 10 South Korean papers in 2002, 7 were presented through this combination. ISRC is a semiconductor research facility established in 1989 within the site of Seoul National University and jointly owned by several universities. It also serves as an industry-academic joint research center. If more universities use ISRC in the future, the number of South Korean papers may further increase.

3.6 Conclusion

It has been learned through the conferences that individual technologies for the 65nm and later generations are steadily advancing. In addition, it is gradually becoming clear which of the technologies will be the mainstay in those areas where there are multiple-technology options such as lithography. However, it appears that a favorite has yet to be determined. If the technologies to be used are not determined in the coming 2 years or so for starting production of 65nm-generation devices in 2007 as planned in the roadmap, the building of LSI designing and manufacturing lines may not be completed in time.

Concerning the numbers of papers by country, presentations by South Korea and Taiwan are increasing. In the future, it is expected that presentations from China will also increase, and the presence of Asia will further grow.

Glossary

* 1 High-dielectric constant (High-k) gate insulation film

With the FET (Filed-Effect Transistor), which is currently the mainstay transistor, a channel area is established between two electrodes called source and drain, and electric charge is generated in the channel area by inserting a gate insulation film between the source and drain, and applying voltage from the gate electrode to pass an electric current between the source and drain. MOS (Metal-Oxide Semiconductor) FET has the gate electrode, gate insulation film and channel, which are made of metal, oxide and semiconductor, respectively. It is one of the most representative semiconductor devices. CMOS (Complementary MOS) has p-type and n-type semiconductors called pMOS and nMOS, and uses the 2 MOSs to form a logic circuit. As MOS FET becomes miniaturized, its channel also becomes smaller. Therefore, it is necessary to generate much electric charge in the channel by thinning the gate insulation film in order to gain a sufficient ON-stage current. However, with SiO_2, which represents the gate insulation film today, when the film thickness becomes below 1nm, a gate leakage current increases due to the film's flaw or electron tunneling. Accordingly, the use of high dielectric constant materials such as SiON and HfO_2 is being studied as materials for gate insulation films that allow generation of sufficient electric charge in the channel and reduce a leakage current.

* 2 Low-dielectric constant (Low-k) insulation film

As LSI speeds up, the time a signal takes to travel through a wiring has become problematic. Therefore, using a low-dielectric constant insulation film in place of SiO_2 for insulation films around wirings is being studied in order to increase the transmission speed of signals. Currently, research is being conducted in organic compound materials and porous materials.

* 3 SOI

When forming LSI on an ordinary Si wafer, it will cause surplus power consumption or decrease speed since the wafer itself has conductivity. SOI (Silicon on Insulator) eliminates the negative impact of the wafer by affixing a thin wafer (0.5 – 100μm) on an insulated substrate made of glass or the likes, or by forming a silicon-oxide insulation film inside the wafer.

* 4 Next-generation lithography

At present, excimer laser (wavelength: 193nm) that uses argon and fluorine gas (ArF) is used as the light source for lithography equipments. Next-generation lithography equipments after the 65nm

generation use light sources that emit shorter-wavelength lights in order to increase resolution. Currently, F_2 excimer laser (wavelength: 153nm) using fluorine gas (F_2) in place of ArF, EUV (wavelength: 13nm) using metal gas plasmas, and EPL (variable wavelength) using electron beam with mask projection method are among the major candidates. While each method has an advantage and disadvantage, F_2 has been the prime candidate. Other future technologies include an X-ray lithography equipment (its development has almost halted) and LEEPLE (unlike EPL that uses reduced projection, it is an electron beam lithography equipment that uses equally magnified contact masks, and is being developed by Japanese ventures and backed by NTT and Sony).

* 5 Next-generation memory

The current memories include: SRAM (Static Random Access Memory), which is high-speed and used in processors and cache memories; DRAM (Dynamic RAM), which is relatively fast and used as the main memory; flash memory, which is slightly slow in writing and erasing but is non-volatile (stored data remains even after the power is turned off); and hard disc and optical disc, which are slow but have large capacities, in descending order. The next-generation memory requires such properties as non-volatility, high speed and low power consumption to replace DRAM and the others that follow DRAM. Magnetic memory (MRAM) uses magnetism to store data as with the hard disk. Ferroelectric RAM (FeRAM) uses ferrodielectrics' property that enables electric charge excited by voltage to remain even after the voltage is turned off. Other methods include OUM (under development by Ovonyx, a venture financed by Intel), which uses a phase-changing substance whose electric resistance changes between the crystal and amorphous states.

* 6 MEMS

This stands for Micro-Electro-Mechanical Systems. Each MEMS chip uses a micro-fabrication technology, based on semiconductor manufacturing technologies, to contain movable parts measuring around some nanometers to millimeters, and microcircuits. They are also called "micro machines."

* 7 Selete

This stands for Semiconductor Leading Edge Technologies, Inc. It is a joint research union established in 1996 mainly by Japanese semiconductor manufacturers. At the beginning, the union conducted evaluation and standardization of devices that support 300mm wafers. Currently, it conducts research into semiconductor manufacturing technologies for the 65nm and later generations.

* 8 ASET

This is the abbreviation for the Association of Super-Advanced Electronics Technologies. ASET is a joint research union for semiconductor technologies, consisting of more than 10 semiconductor-related companies in Japan. MIRAI is a joint development project for the 65nm generation conducted by ASET.

* 9 Calcium fluoride lens

Since ordinary glass or quartz cannot be used as lens material for the F_2 excimer laser, which emmits at very short wavelength, a calcium fluoride (CaF_2, also called "fluorite") lens is used instead. However, calcium fluoride has disadvantages such as complex refraction (refraction fluctuates according to the crystal azimuth, which is disadvantageous for a lens), low mechanical strength so causes deformation of lens due to weight of itself.

*10 IMEC

IMEC is an academic-business-government semiconductor research center jointly managed by the Belgian kingdom's Flanders provincial government, 4 universities in the province and semiconductor-related companies.

*11 CEA

This stands for "Commissariat a l'Energie Atomique," the French atomic energy commission.It has the research institute for LSI technologies and nanotechnologies.

(Original Japanese version: published in July 2002)